TEXAS DEPARTMENT OF TRANSPORTATION
DEPARTMENTAL SPECIFICATION
BUS INTERFACE UNIT (BIU) TESTER
TO-6000

1.0 SCOPE

1.1 This specification sets forth the minimum requirements for a NEMA TS2 Bus Interface Unit (BIU) tester.

2.0 GENERAL

2.1 The BIU tester shall be designed to run a complete set of standards based tests on timing and functions as defined in the NEMA TS-2 1998 standards.

2.2 The tester shall include all hardware, firmware, cabling and accessories required to test a NEMA TS2 BIU and save a test report to the tester's memory. The tester shall be capable of downloading saved test reports via RS232.

3.0 BIU TESTER DESCRIPTION

3.1 The tester shall provide the proper DIN connector and guides to connect with the BIU back-plane connector, providing power and I/O connections. The tester shall provide the 15-pin D sub cable to interface with the SDLC connector on the front panel of the BIU. The tester shall also test the I/O and SDLC communications.

3.2 The tester shall provide a standard 9-pin D-sub RS232 port for serial data transmission of test reports to the compact printer or a compatible computer.

3.3 The tester shall operate on 120 VAC 60 Hz power. The tester shall have adequate overcurrent protection.

3.4 The tester manufacturer shall make available a compact printer, which fits inside the tester enclosure, which can be used to printer test reports in the field.

3.5 The tester shall include a multi-function keypad which allows operator input of BIU model, serial number, comments, and operator ID which are then saved by the tester, along with the time and date and test results to form a test report. The tester shall also include a multi-line alphanumeric display to prompt the operator during the test setup and provide feedback for manual data entry.

3.6 The tester shall be housed in an impact-resistant suitcase-style enclosure, which contains and protects all components of the tester. The enclosure shall contain the tester, power cord, compact printer, printer cable, SDLC communication cable, and Operating Manual. The tester enclosure shall not exceed 15 in. X 20 in. X 5 in. The weight of the tester shall not exceed 14 lbs.

4.0 BIU Test Descriptions

4.1 BIU set to Address 0 (TF #1). The 24 V supply power is set to 0 V for 10,000 mS, then restored. The BIU is then repeatedly polled. The state of the output pins should be pulled high within 100 mS from the point in time when 16 V was achieved by the power supply. (Standard: All outputs active within 100 mS of power-on state).

4.2 Part 1: BIU set to Address 0 (TF #1) and all output pins are asserted. The 24 V supply power is set to 0 V for 700 mS, then restored. The state of the ouput pins should remain in the asserted state.
Part 2: Same as Part 1, except input power is set to 15.8 V instead of 0 V. (Standard: BIU shall operate through a 700 mS power loss. Power loss is anything less than 16 V applied to the device).

4.3 BIU set to Address 0 (TF #1) and all output pins are asserted. The 24 V supply power is set to 0 V for 1500 mS, then restored. The state of the output pins should revert to the un-asserted state. (Standard: BIU shall reset upon a > 1500 mS power loss).

4.4 BIU is set to each of the eight detectors and T&F addresses in sequence. Appropriate command frames are sent to each address while valid. The response of the IU will confirm the proper status. (Standard: Proper response frame returned by BIU)

4.5 BIU set to address 8 (DET #1). Tester sends a command frame pair to the BIU 100 times in 10 seconds. BIU should respond with the correct frame 100 times.

4.6 BIU set to address 0 (T&F #1). Tester sends a command frame with a built-in error. The BIU should not respond to the test frame.

4.7 BIU set to address 0 (TF #1). DC pulses are applied to Opto input #1 for increasingly longer time periods, starting from 100 mS and up through 100 mS. Between each test input the BIU is polled to see when the input is recognized. (Standard: 50 mS or more must be recognized, less than 25 mS must be ignored).

4.8 BIU is set to address 8 (DET #1). Pulses of steadily increasing widths are applied to the detector inputs until the input is recognized by the BIU. The tester records the minimum pulse width for recognition. (Standard: .25 mS to 1.0 mS).

4.9 BIU is set to address 0 (T&F #1) with all pins un-asserted (pulled to 24 V). Each input pin is pulled down by the tester to 7 V and then 17 V and BIU is polled to determine the state of the inputs. (Standard: Input becomes asserted between 16 V and 8 V).

4.10 BIU is set to address 0 (T&F #1). A sine wave is applied to the pin at 60 Hz, with steadily increasing amplitude until the input is seen as asserted by the BIU.

4.11 BIU is set to addresses 0 through 3 (T&F #1 through 4). Bi-directional current pulses are applied to the opto inputs to change their state. The BIU is polled to verify their response. (Standard: Inputs should respond to bi-directional current inputs).

4.12 BIU is set to each of the four detector addresses in sequence. The proper command frame (type 24 to 27) is sent to the BIU. The BIU reset outputs should be asserted following the receipt of the frame. (Standard: Reset frame functions).

4.13 BIU is set to each of the four detector addresses in sequence. Calls are placed, then removed on each of the input pins and the BIU is polled to confirm their status. (Standard: 16 detector channels per BIU)

4.14 BIU is set to each of the four detector addresses in sequence. Each detector input is tested with 5 Pulse-Width-Modulated (PWM) status messages. The BIU is polled to verify that it can interpret the signals correctly (320 tests). (Standard: BIU should interpret 5 PWM codes for the controller).

4.15 BIU is set to each of the four T&F addresses in sequence. Tester sends a command frame and an output transfer frame in sequence to set the BIU outputs. The tester checks the output pins to confirm the proper status.

4.16 BIU is set to TF #1 and TF #2 addresses in sequence. Tester sends a command frame in sequence to drive the load switch in each of the four output states: Off, On, +Half Wave, -Half Wave. The Line Frequency Reference signal is removed from the input, and the BIU is sent another series of frames to test each output state. The tester checks the output pins to confirm proper operation.

4.17 BIU is set to each of the four T&F addresses in sequence. Tester drives the input pins high and low and sends a command frame for each state to verify the BIU reads the inputs properly.

4.18 BIU is set to address 0 (T&F #1). Tester sends a frame to establish the pending state of the output pins. Tester then sends a transfer frame (type 18). BIU is polled repeatedly after receipt of the type 18 frame to verify the state of the output pins. (Standard: Outputs must change state within 20 mS).

4.19 BIU is set to addresses 0 (T&F #1). Tester applies a short (7 mS) and a long (25 mS) pulse to the inputs to change their state. The BIU is polled to verify their response. (Standard: Inputs should ignore 7 mS and accept 25 mS).

4.20 BIU set to Address 0 (TF #1). The BIU is powered up and polled to initiate communication. The SDLC clock pulse signal is monitored and measured to determine the frequency, duty cycle, and position of the clock edge within the bit cell. (Standard: Frequency is 153600 Hz +/-1%, Duty cycle is 50% +/-1%, Clock Edge is Midpoint of Bid Cell +/-10%).

4.21 BIU set to address 0 (TF #1). The BIU is powered up and the line frequency signal applied to the input. The input signal is tested for the requisite impedance to 24 VDC, and that the proper rise and fall times are ensured.

5.0 Warranty

5.1 The tester shall be protected by a one-year limited warranty on parts and labor. The continuing utility of the tester shall be further protected by the availability of repair, update, recalibration, and extended warranty services from the manufacturer.